Document Number: EDCS-874867

Revision: 02

Originator: Phong Trinh/Matt Di Paola

Dept: Structural Test

**ICT Program Review Check List for A3070**

**Approvals**

|  |  |  |
| --- | --- | --- |
| Department | Name | Approval Date |
| Structural Test | Lap Le | MM/DD/YYYY |
| Structural Test | John Huang | MM/DD/YYYY |

**Modification History**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Rev | RCN # | Date | Originator | Comments |
| 01 |  |  |  |  |
| 02 |  |  |  |  |

**PURPOSE:**

This document provides Structural Test Engineers guidelines to review an ICT program. This review includes the test coverage report, board file and ICT program testplan.

**SCOPE:**

Described in this document are various review documents such as the test coverage report, board file and ICT program testplan in which the STE needs to review to release the ICT test program to production.

**DEFINITION:**

STE Structural Test Engineer

ICT In Circuit Test

CPN Cisco Part Number

MPa Manufacturing Partner

bdg Board Grading

PCAMAP Printed Circuit Assembly Manufacturing Assembly Procedure

|  |  |
| --- | --- |
| **Board Name** | Churchill CPU |
| **CPN** | 73-19882-04 |
| **MPa** | Foxconn |
| **STE Name** | Kevin Nguyen |
| **Date** | 2020/09/23 |

* 1. Review TestCoverage report file
* a) Review posted ICT test time.

 

146.8s

* b) Review and approve the Test-Gap report provided by MPa.

 

* c) Review no value added vectorless tests and remove from test.

 

* 2. Review Testplan File
* a) Review that the testplan header is completely filled out with all Cisco required info. ( See Appendix A)



* b) Review the power-up subroutine is consistent with the power up sequence provided by the board designer

 

* c) Review that the clocks are not shut down during the power up sequence of the board.

 

* d) Review that no gp-relay connections are active during the board power up sequence unless recommended by the power up sequence supplied by the board designer.

 

* e) Review that there is no power supply cycling thorough the testplan.

 

* f) Review that all power rails or tested immediately following the power up sequence.

 

* g) Review that the boundary scan bus wire test (\*\_bus) is executed.

 

* 3. Review Board file
* a) Review that all nodes in the fixed node section are true fixed nodes.

 

* b) Review that the Family Options section voltage levels dh, dl, rh and rl are all defined correctly for each voltage family.

 

* 4. Review Analog Unpower tests
* a) Review all diode tests and insure idc is a minimum of 10mA.

 

* b) Review all LED tests and insure idc is a minimum of 20mA.

 

* c) Review that all transistors and FETs use the powered test (Chay Transistor/FET power test).

 

All Chay Transistor were not used powered test.

* d) Review that no capacitors with a value less then 20pF are tested.

 

All capacitors less than 30pf are not tested.

* e) Review that all inductors with a value greater than 1 mH are tested for the inductance value.

 

No inductor greater than 1mH.

* f) Review that in all resistor and capacitor tests the I bus is connected to the non power rail net.

 

* g) Review that all header type connectors are tested using a presence switch.

 

* 5. Review Analog Powered + Mixed + Sensor-LED tests
* a) Review that no formulas or calculations are done internal to analog tests.

 

* b) Review that all Xtal devices that can be tested indirectly are tested using a downstream device and clock divider.

 

* c) Review that all Oscillators greater than 60 Mhz must have a clock divider with +/- 5% tolerance.

 

* 6. Review Digital tests
* a) Review that all digital tests called in the testplan exercise a minimum of one pin. The test is in the testplan, but doing nothing.

 

* 7. Review Boundary Scan tests
* a) Review that there is only one boundary scan chain.

 

* b) Review all boundary scan tests to insure no pins are commented.

 

Pls refer to the “TC\_comment for Churchill CPU” folder directory under docs of the program.

* c) Review that no boundary scan devices are in bypass mode.

The PFBGA should be in this mode in chain, or it will cause power down.

 

* 8. Review BDG data files
* a) Review the vacuum off tests and insure that all tests fail.

 

* b) Review the vacuum on tests and insure that all tests pass.

 

* c) Review that all the bdg data has been generated including the data for vectorless test and boundary scan.

 

* 9. Other …
* a) Review and approve the probe removal list provided by MPa. (See appendix B)

 

* b) Review that all nets with pulled or removed probes have been updated in the fixture files.

 

* c) Shorting Plate tests – Recommended for debug purpose.

Use the short& open board to verify the fixture before we debug the board.

 

* d) ICT fixture photos.

Pls refer to the fixture photo folder directory under docs of the program.

 

* 10. Control run before release to production
* a) Pick minimum 5 good boards from the current build.

 

This action will be finished in FAI process.

* b) Run ICT test minimum 5 times on each board.

 

This action will be finished in FAI process.

* c) During the control run, if a board fails, identify the root cause and make the corrective action before proceeding to test the rest of the boards.

 

This action will be finished in FAI process.

* d) All passed boards must complete the entire required test process.

 

This action will be finished in FAI process.

Appendix A: Testplan header format.

File Name :

Assembly Name :

Board Name :

Fab : 28-XXXX-XX Rev xx

Bom : 73-XXXXX-XX Rev xx

Schematic : 92-xxxx-xx Rev xx

PCA Map : 61-xxxx-xx Rev xx

CM Test Engineer :

Last Update : mm/dd/yy

ICT board S/N :

Cisco Fixture Asset Tag :

Installation Date : mm/dd/yy

CM :

Appendix B: Probes removal list format.

Netname Connections Comments

MEM\_D1 U1.3, U2.5, R100.1

PLD\_RST U5.A1, U3.F2